

US005438519A

United States Patent [19]

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[11] Patent Number:

5,438,519

[45] Date of Patent:

Aug. 1, 1995

[54] ELECTRONIC POSTAGE METER HAVING MEMORY WRITE ACCESS SECOND CHANCE HARD TIMER MEANS

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[21] Appl. No.: 989,673

[22] Filed: Feb. 10, 1993

918.52, 950, 950.4

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[57] ABSTRACT

A postage meter control system includes a microcomputer having a programmable microprocessor. The microcomputer is in communication with a decoder integrated circuit (Decoder IC). The Decoder IC has a first write control flip-flop and a second write control flip-flop, as in the preferred embodiment there are redundant non-volatile memories. Each control flip-flop has an output to a respective AND gate. The Decoder IC includes a dual timer which has an output to the control flip-flops. As a result, when the microcomputer enters write routine, the timer releases the control flipflops to allow the system to be write enabled. If the write routine encounters a error, resulting in the timer timing out, the timer resets the control flip-flop and communicates with the microcomputer to try a retry. A more detailed description, and other features and advantages will become apparent in conjunction with the detailed description of the preferred embodiment.

1 Claim, 22 Drawing Sheets

